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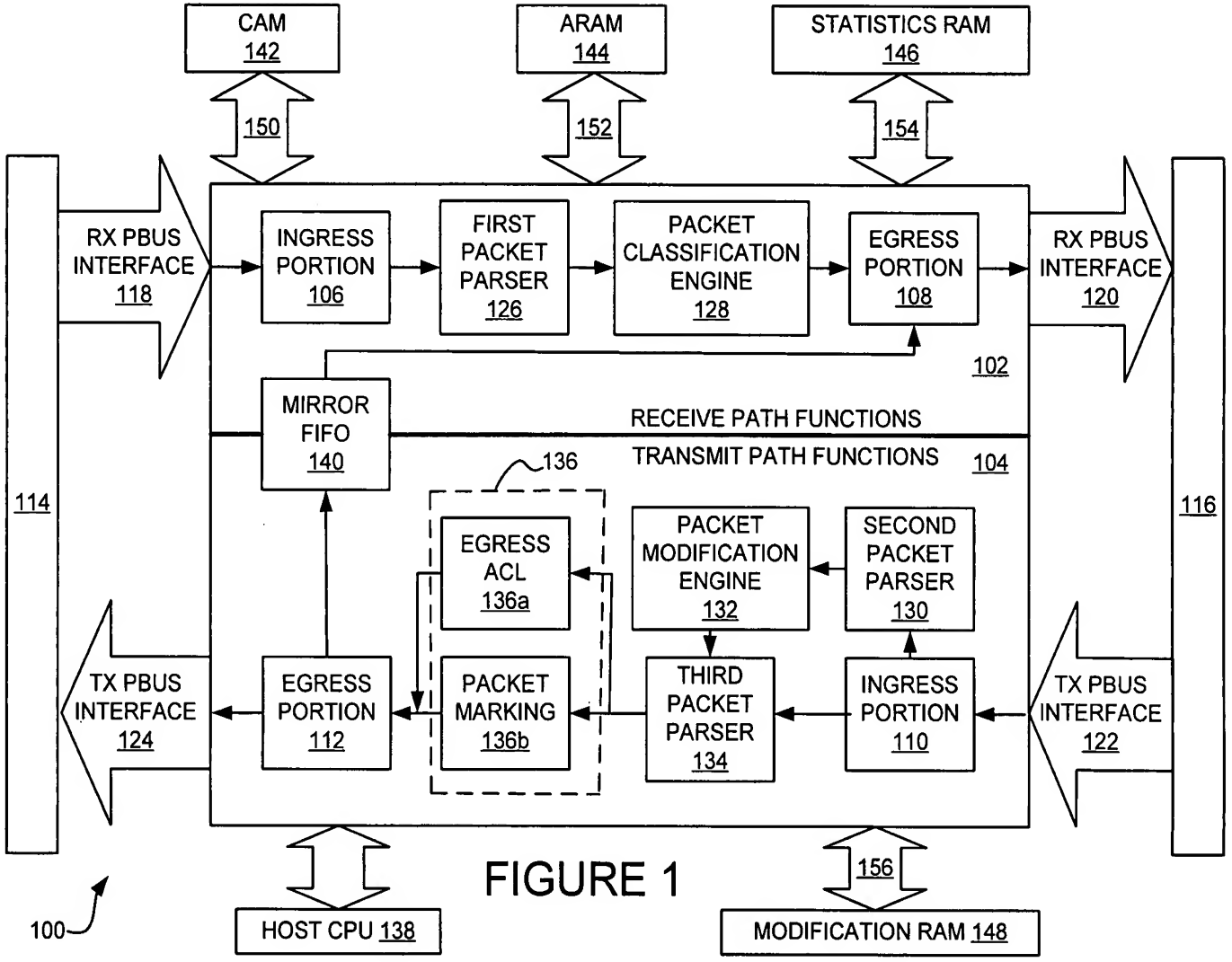
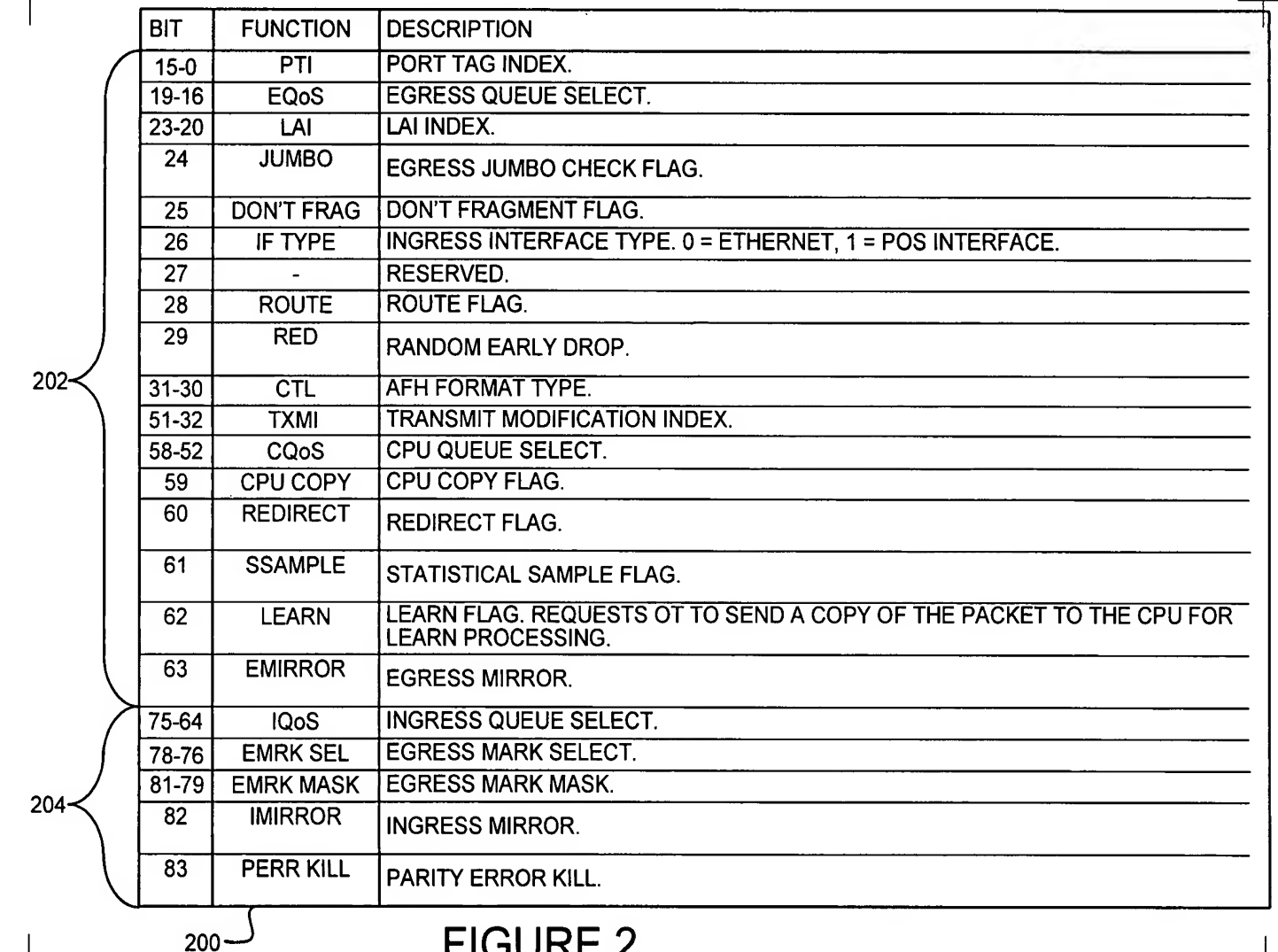

CAM
142
ARAM
144
STATISTICS RAM
146
150
152
154
RX PBUS
INTERFACE
118
INGRESS
PORTION
106
FIRST
PACKET
PARSER
126
PACKET
CLASSIFICATION
ENGINE
128
EGRESS
PORTION
108
RX PBUS
INTERFACE
120
102
MIRROR
FIFO
140
RECEIVE PATH FUNCTIONS
TRANSMIT PATH FUNCTIONS
104
136
114
116
EGRESS
ACL
136a
PACKET
MODIFICATION
ENGINE
132
SECOND
PACKET
PARSER
130
TX PBUS
INTERFACE
124
EGRESS
PORTION
112
PACKET
MARKING
136b
THIRD
PACKET
PARSER
134
INGRESS
PORTION
110
TX PBUS
INTERFACE
122
100
HOST CPU 138
156
MODIFICATION RAM 148

FIGURE 1



BIT	FUNCTION	DESCRIPTION
15-0	PTI	PORT TAG INDEX.
19-16	EQoS	EGRESS QUEUE SELECT.
23-20	LAI	LAI INDEX.
24	JUMBO	EGRESS JUMBO CHECK FLAG.
25	DON'T FRAG	DON'T FRAGMENT FLAG.
26	IF TYPE	INGRESS INTERFACE TYPE. 0 = ETHERNET, 1 = POS INTERFACE.
27	-	RESERVED.
28	ROUTE	ROUTE FLAG.
29	RED	RANDOM EARLY DROP.
31-30	CTL	AFH FORMAT TYPE.
51-32	TXMI	TRANSMIT MODIFICATION INDEX.
58-52	CQoS	CPU QUEUE SELECT.
59	CPU COPY	CPU COPY FLAG.
60	REDIRECT	REDIRECT FLAG.
61	SSAMPLE	STATISTICAL SAMPLE FLAG.
62	LEARN	LEARN FLAG. REQUESTS OT TO SEND A COPY OF THE PACKET TO THE CPU FOR LEARN PROCESSING.
63	EMIRROR	EGRESS MIRROR.
75-64	IQoS	INGRESS QUEUE SELECT.
78-76	EMRK SEL	EGRESS MARK SELECT.
81-79	EMRK MASK	EGRESS MARK MASK.
82	IMIRROR	INGRESS MIRROR.
83	PERR KILL	PARITY ERROR KILL.

FIGURE 2

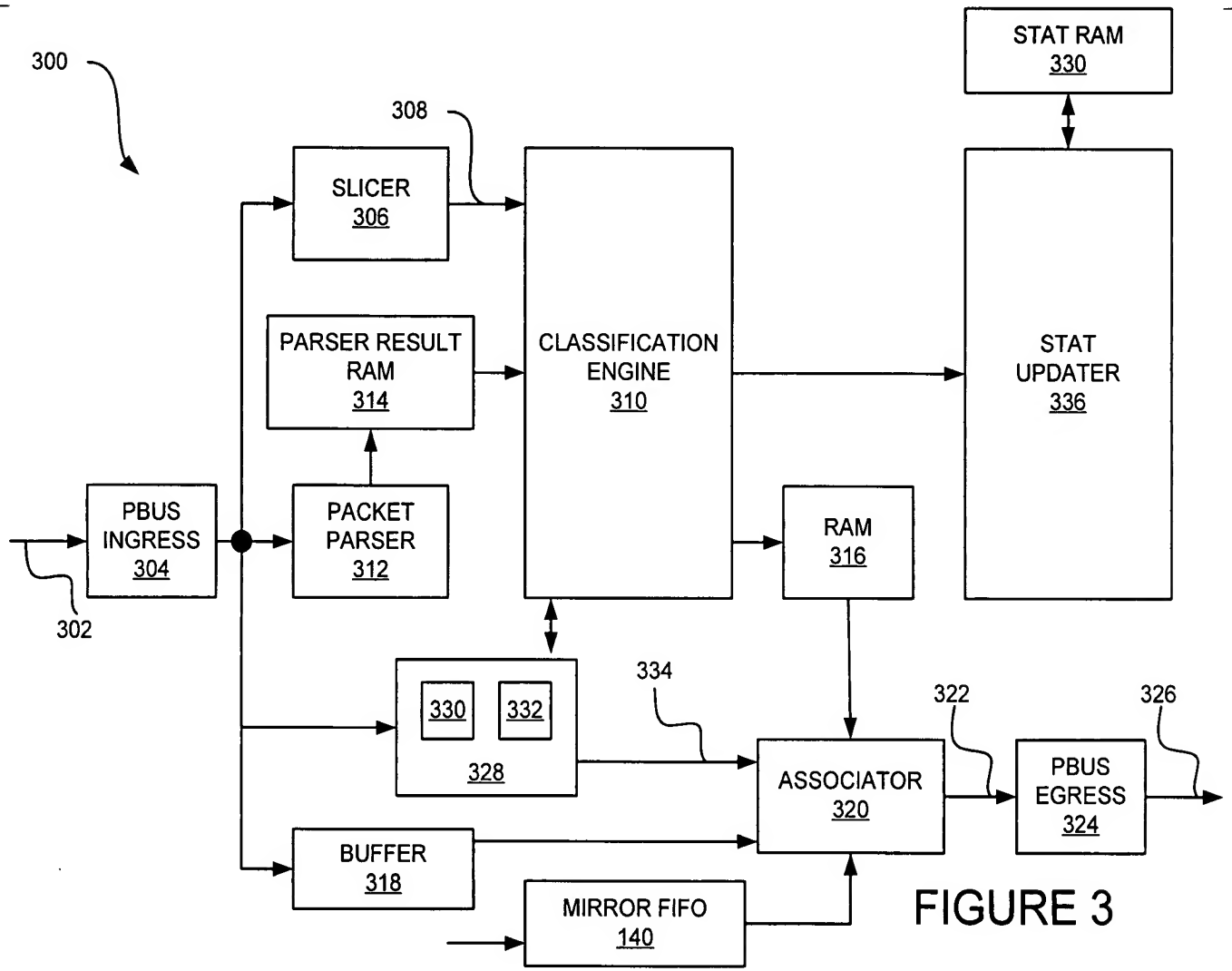

300
308
SLICER
306
STAT RAM
330
PARSER RESULT
RAM
314
CLASSIFICATION
ENGINE
310
STAT
UPDATER
336
PBUS
INGRESS
304
PACKET
PARSER
312
RAM
316
302
330
332
328
334
322
326
ASSOCIATOR
320
PBUS
EGRESS
324
BUFFER
318
MIRROR FIFO
140

FIGURE 3

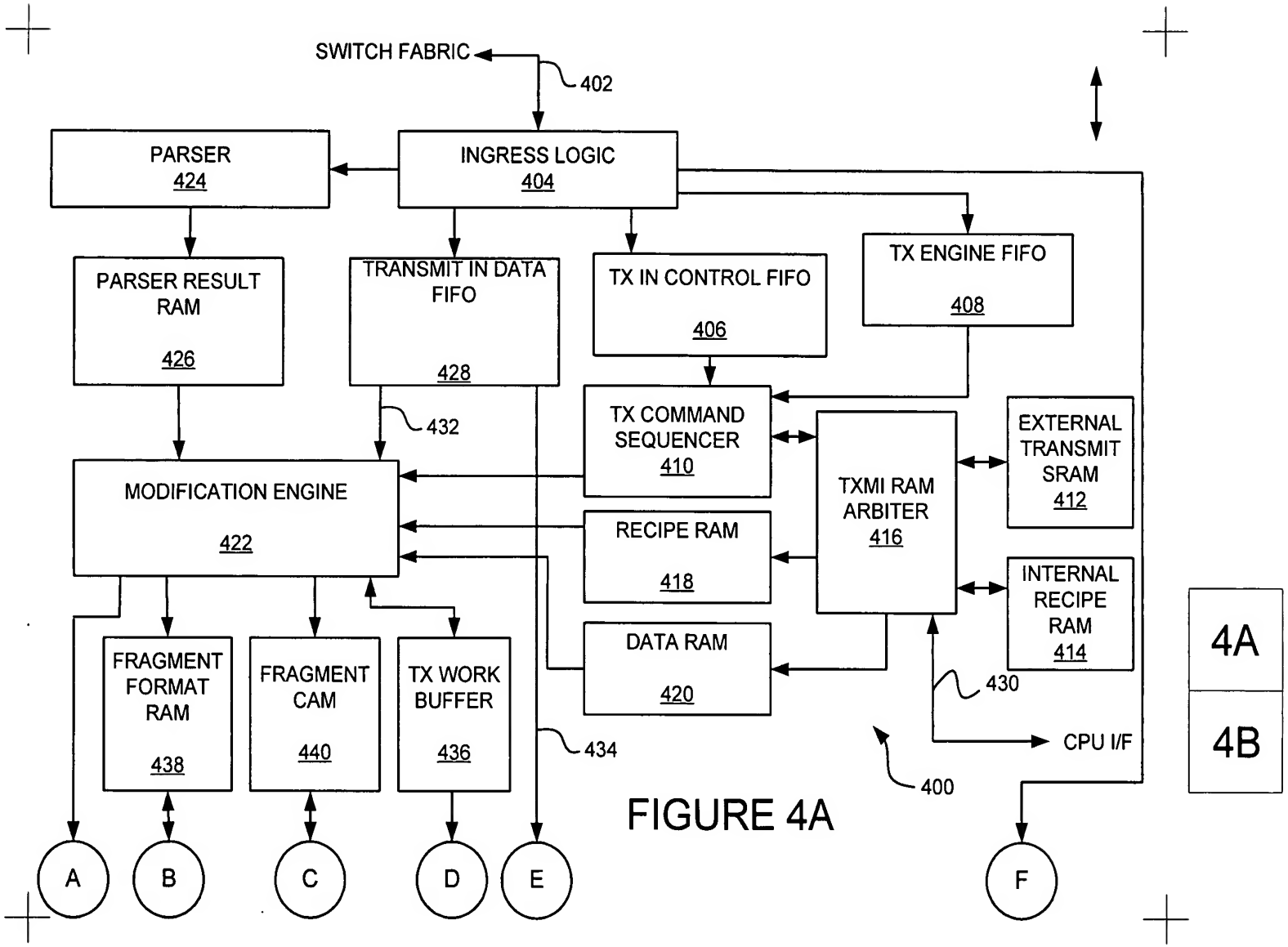

SWITCH FABRIC
402
PARSER
424
INGRESS LOGIC
404
PARSER RESULT RAM
426
TRANSMIT IN DATA FIFO
428
TX IN CONTROL FIFO
406
TX ENGINE FIFO
408
432
TX COMMAND SEQUENCER
410
TXMI RAM ARBITER
416
EXTERNAL TRANSMIT SRAM
412
MODIFICATION ENGINE
422
RECIPE RAM
418
INTERNAL RECIPE RAM
414
DATA RAM
420
430
FRAGMENT FORMAT RAM
438
FRAGMENT CAM
440
TX WORK BUFFER
436
434
CPU I/F
400
A
B
C
D
E
F
4A
4B

FIGURE 4A

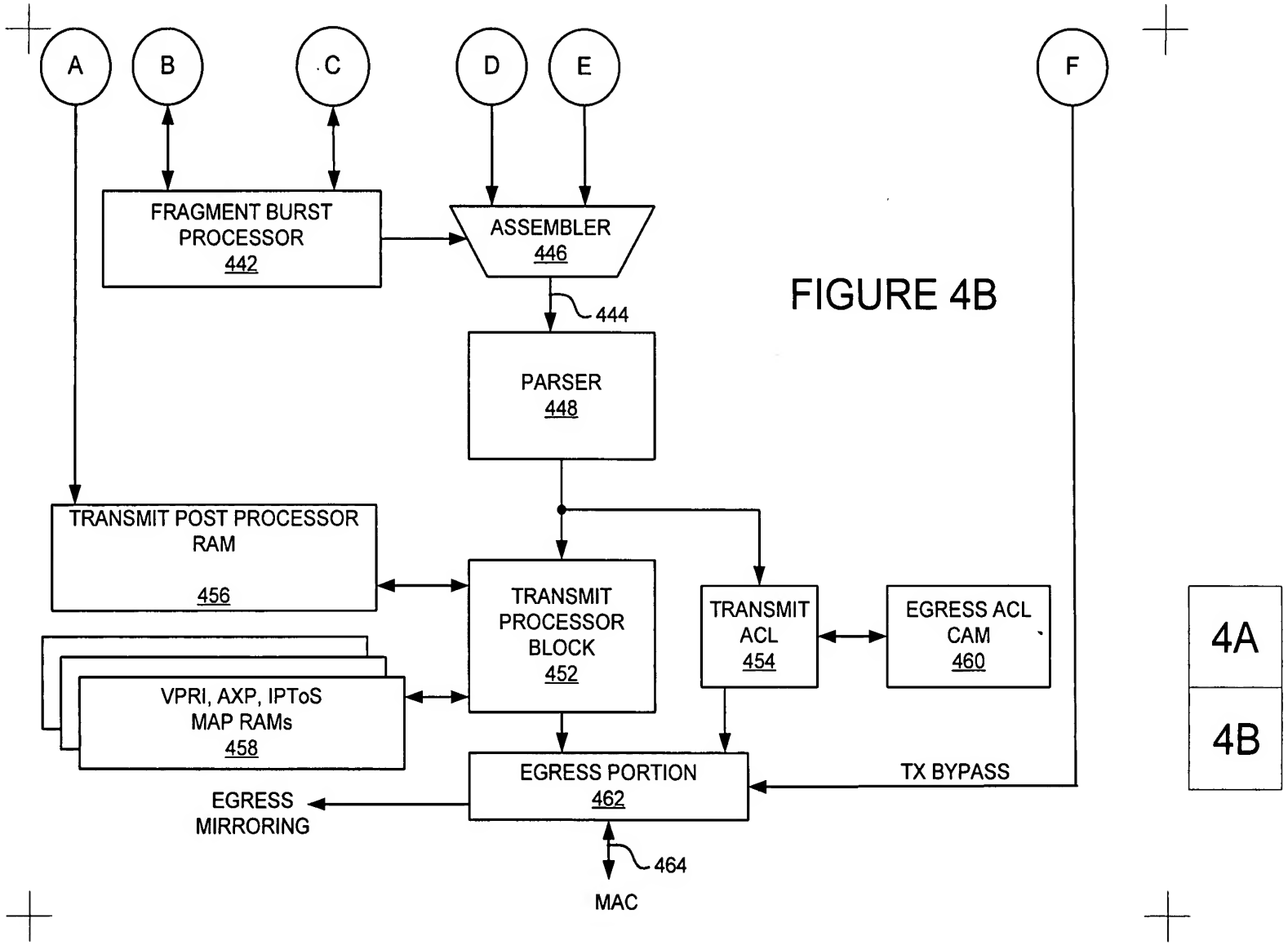

A
B
C
D
E
F
FRAGMENT BURST PROCESSOR 442
ASSEMBLER 446
444
PARSER 448
TRANSMIT POST PROCESSOR RAM 456
TRANSMIT PROCESSOR BLOCK 452
TRANSMIT ACL 454
EGRESS ACL CAM 460
VPRI, AXP, IPToS MAP RAMs 458
EGRESS PORTION 462
TX BYPASS
EGRESS MIRRORING
464
MAC
4A
4B

FIGURE 4B

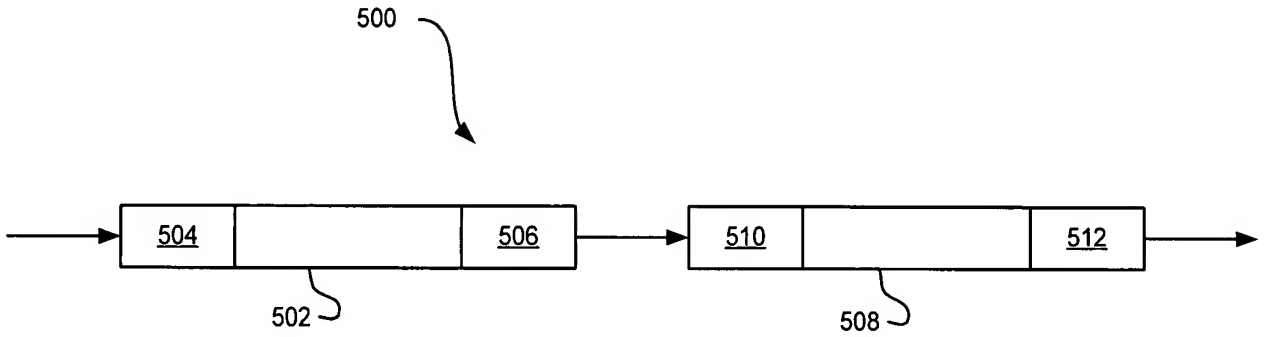


FIGURE 5

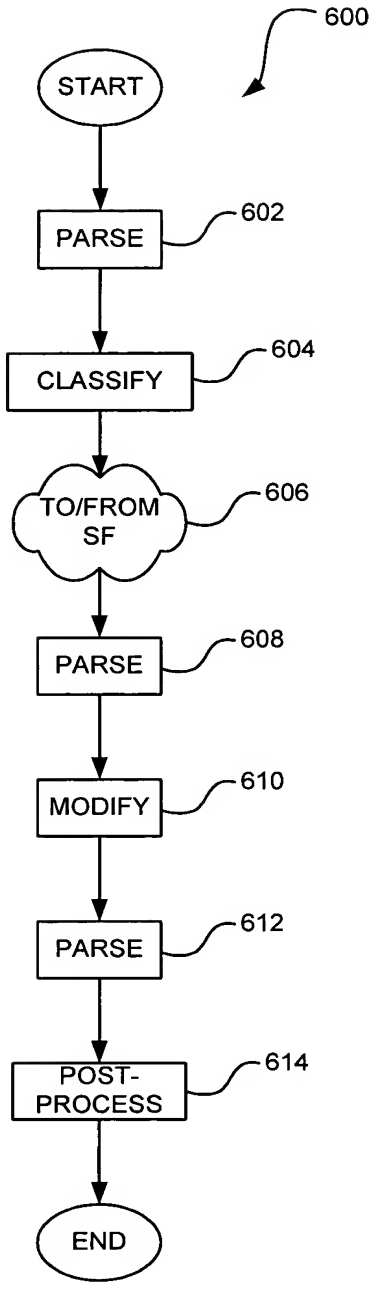

600
START
PARSE
602
CLASSIFY
604
TO/FROM SF
606
PARSE
608
MODIFY
610
PARSE
612
POST-PROCESS
614
END

FIGURE 6

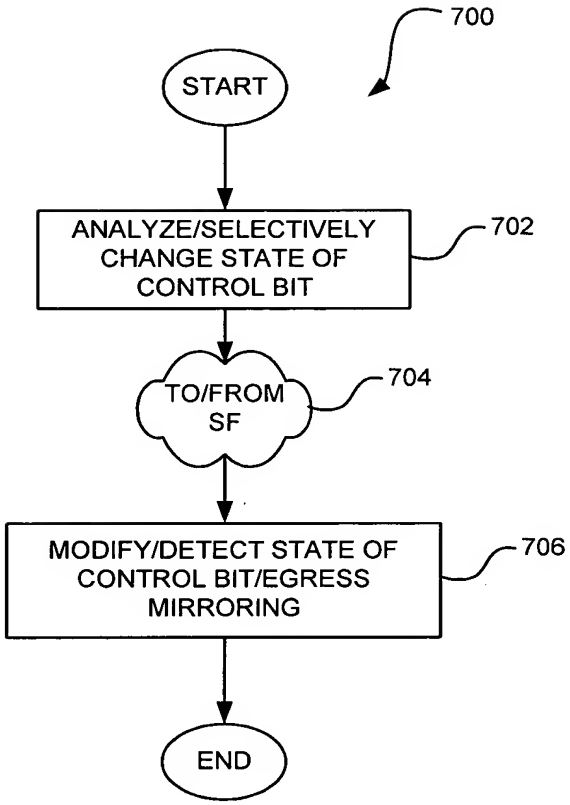

700
START
ANALYZE/SELECTIVELY CHANGE STATE OF CONTROL BIT
702
TO/FROM SF
704
MODIFY/DETECT STATE OF CONTROL BIT/EGRESS MIRRORING
706
END

FIGURE 7

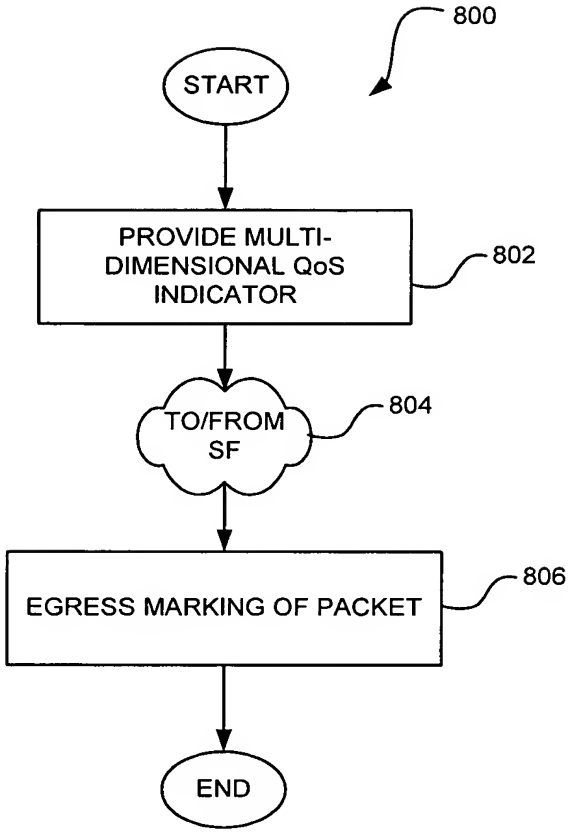

800
START
PROVIDE MULTI-DIMENSIONAL QoS INDICATOR
802
TO/FROM SF
804
EGRESS MARKING OF PACKET
806
END

FIGURE 8

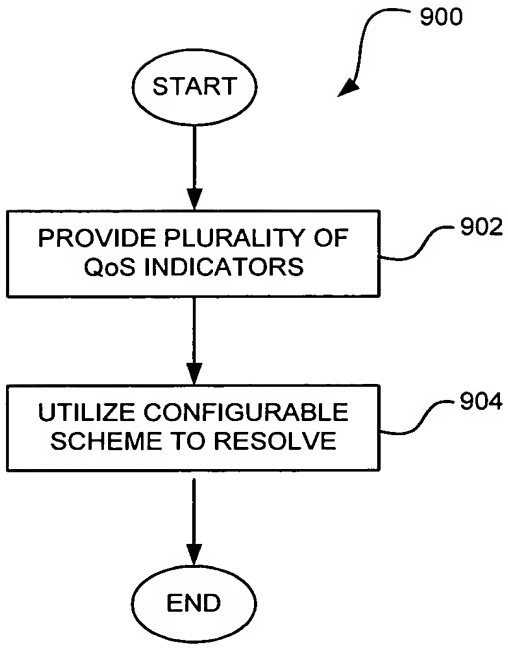

900
START
PROVIDE PLURALITY OF QoS INDICATORS
902
UTILIZE CONFIGURABLE SCHEME TO RESOLVE
904
END

FIGURE 9

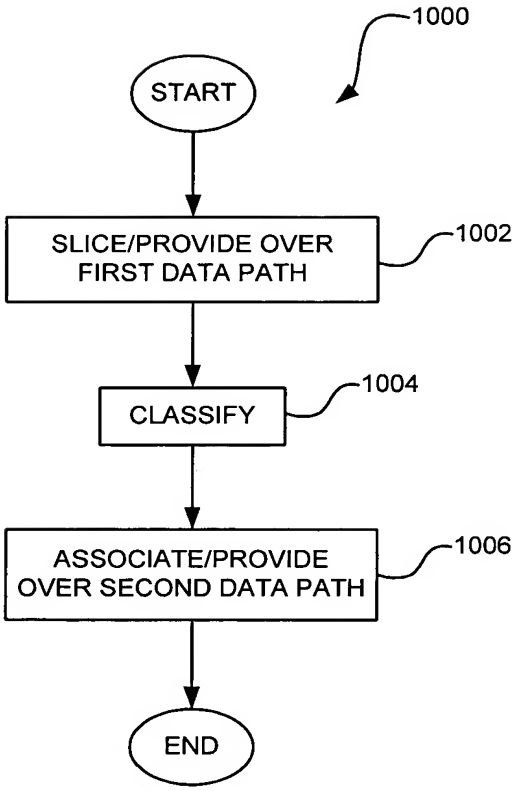

1000
START
SLICE/PROVIDE OVER FIRST DATA PATH
1002
CLASSIFY
1004
ASSOCIATE/PROVIDE OVER SECOND DATA PATH
1006
END

FIGURE 10

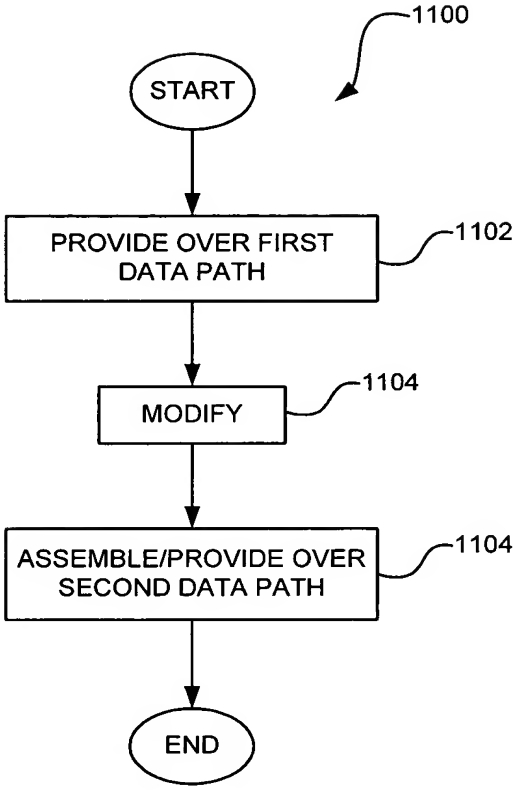

1100
START
PROVIDE OVER FIRST DATA PATH
1102
MODIFY
1104
ASSEMBLE/PROVIDE OVER SECOND DATA PATH
1104
END

FIGURE 11

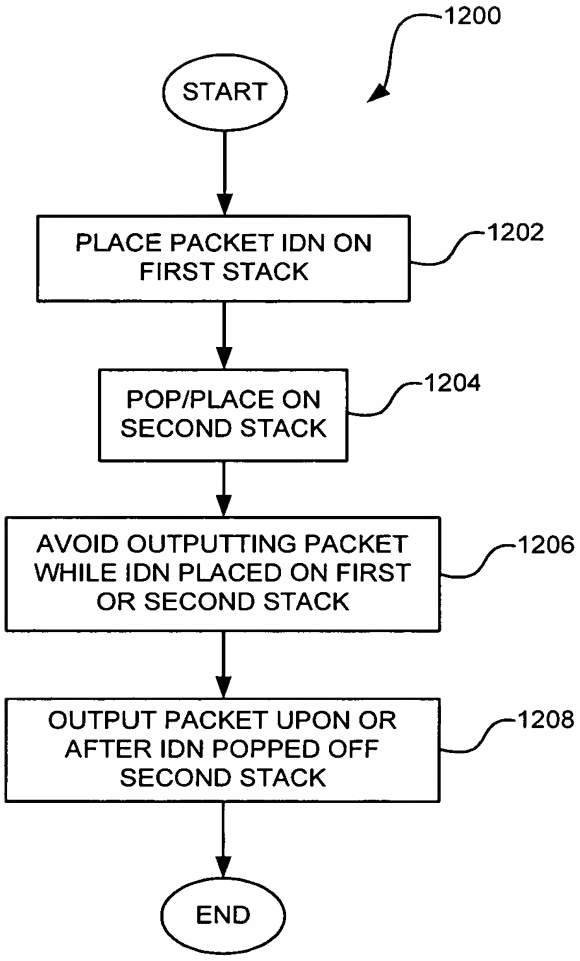

1200
START
PLACE PACKET IDN ON FIRST STACK
1202
POP/PLACE ON SECOND STACK
1204
AVOID OUTPUTTING PACKET WHILE IDN PLACED ON FIRST OR SECOND STACK
1206
OUTPUT PACKET UPON OR AFTER IDN POPPED OFF SECOND STACK
1208
END

FIGURE 12

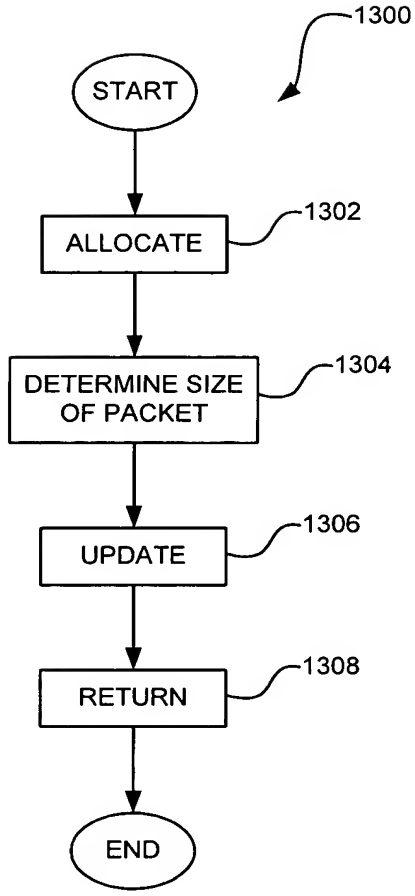

1300
START
ALLOCATE
1302
DETERMINE SIZE OF PACKET
1304
UPDATE
1306
RETURN
1308
END

FIGURE 13

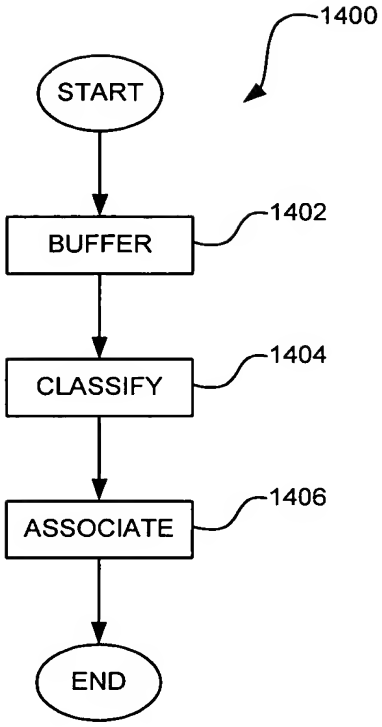


FIGURE 14

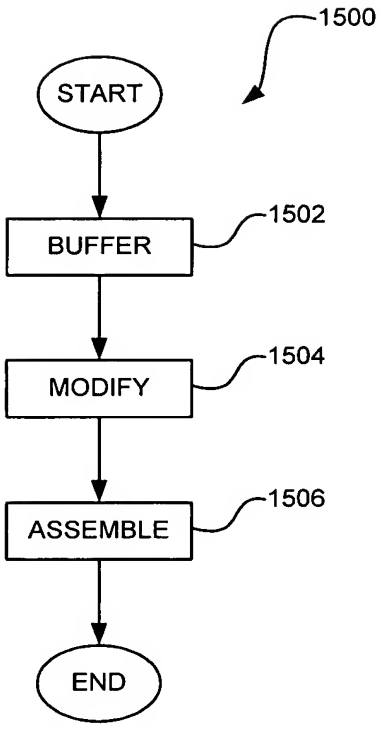


FIGURE 15

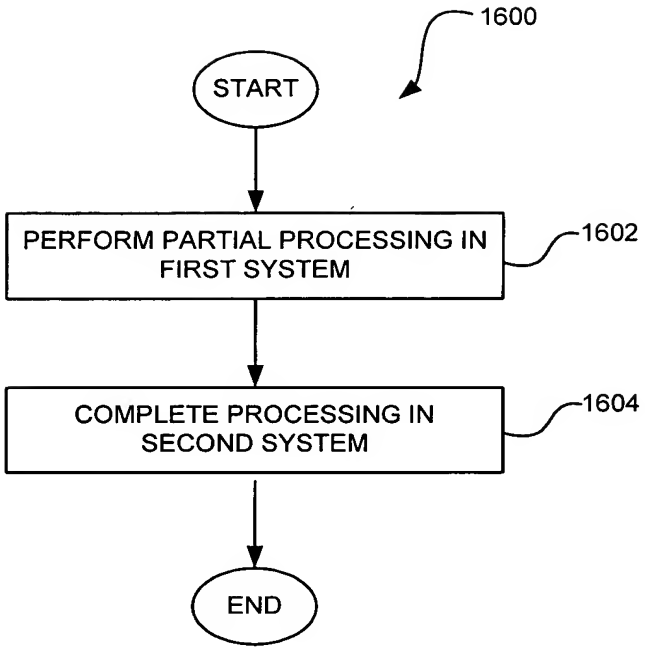

1600
START
PERFORM PARTIAL PROCESSING IN FIRST SYSTEM
1602
COMPLETE PROCESSING IN SECOND SYSTEM
1604
END

FIGURE 16

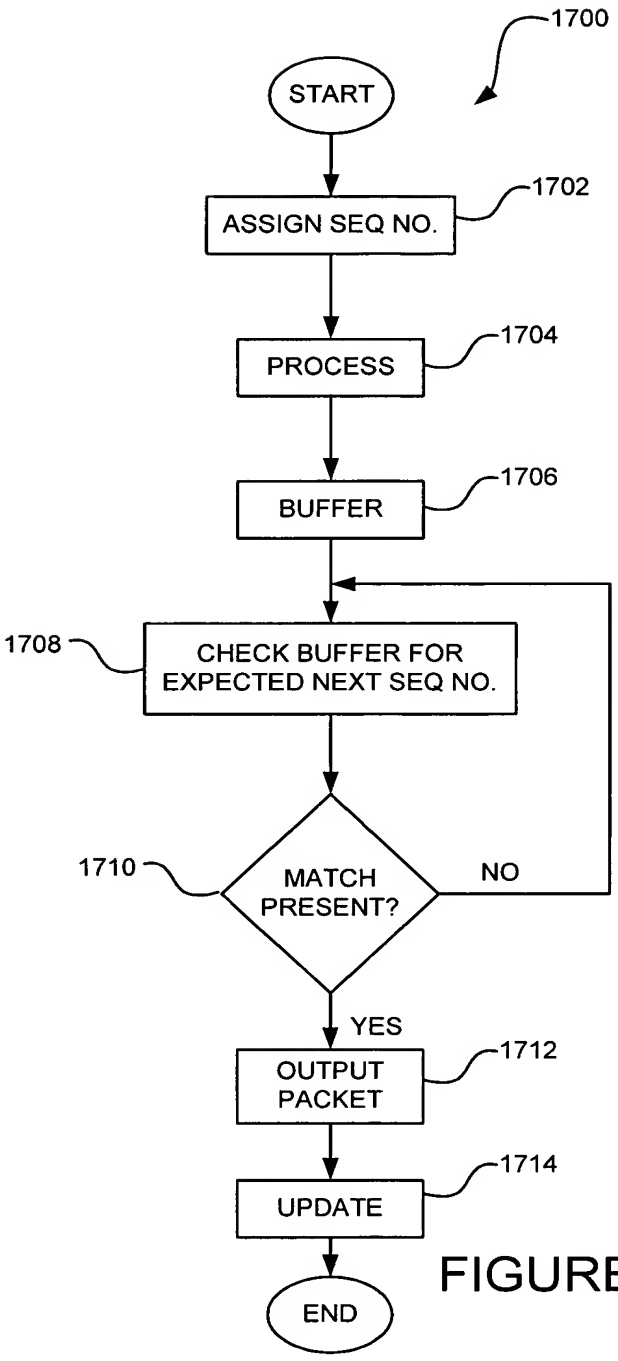

1700
START
1702
ASSIGN SEQ NO.
1704
PROCESS
1706
BUFFER
1708
CHECK BUFFER FOR EXPECTED NEXT SEQ NO.
1710
MATCH PRESENT?
NO
YES
1712
OUTPUT PACKET
1714
UPDATE
END

FIGURE 17

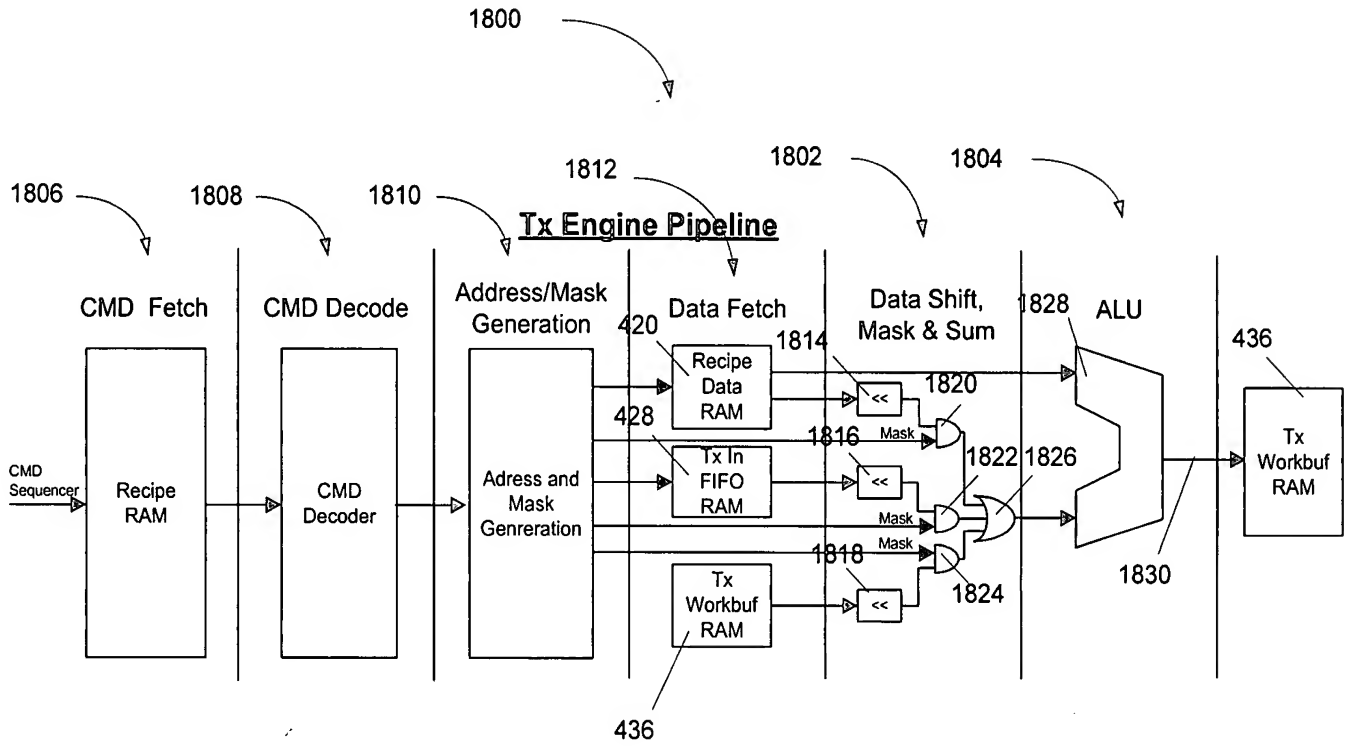

1800
1806
1808
1810
1812
1802
1804
Tx Engine Pipeline
CMD Fetch
CMD Decode
Address/Mask Generation
Data Fetch
Data Shift, Mask & Sum
ALU
CMD Sequencer
Recipe RAM
CMD Decoder
Adress and Mask Genreration
420
Recipe Data RAM
428
Tx In FIFO RAM
Tx Workbuf RAM
436
1814
1816
1818
1820
1822
1824
1826
1828
1830
436
Tx Workbuf RAM
Mask
Mask
Mask
<<
<<
<<

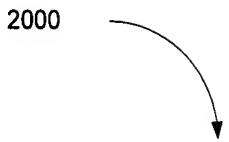
FIGURE 18

1900

10.4.1.1. *External Link Entry Format*

Bit	*Function*	*Description*
17-0	BURST ADDR 0	Burst Address 0.
21-18	BURST LEN 0	Burst Length 0.
41-22	BURST ADDR 1	Burst Address 1.
45-42	BURST LEN 1	Burst Length 1.
65-46	BURST ADDR 2	Burst Address 2.
69-66	BURST LEN 2	Burst Length 2.
70	INT/EXT	Internal/External.
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

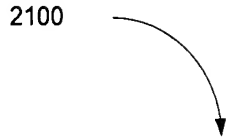
FIGURE 19



10.4.1.2. Internal Link Entry Format

Bit	*Function*	*Description*
20-0	BURST ADDR 1	Burst Address 1.
25-21	BURST LEN 1	Burst Length 1.
46-26	BURST ADDR 2	Burst Address 2.
51-47	BURST LEN 2	Burst Length 2.
62-52	INT RECIPE INDEX	Internal Recipe Index.
67-63	INT RECIPE LEN	Internal Recipe Length.
69-68	-	Reserved.
70	INT/EXT	Internal/External.
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

FIGURE 20



10.4.1.4. Data Entry Format

Bit	*Function*	*Description*
31-0	DATA 0	Data Segment 0.
35-32	DATA LEN	Data Length.
67-36	DATA 1	Data Segment 1.
70-68	-	Reserved.
71	PAR	Parity Bit. Set so that there is odd parity across bits 71:0 of the entry data.

FIGURE 21A


TXM Data/Mask Format inside the external TXM RAM
Parity[71] Reserved[70:68] Mask2[67:60] Data2[59:44] Data1[43:36] Length[3:0] Mask0[31:16] Data0[15:0]
Parity[71] Reserved[70:68] Unused[67:36] Length[3:0] Unused[31:8] Mask2[7:0]

FIGURE 21B

Internal Recipe RAM Data Format				
[71]	[70]	[69:36]	[35:34]	[33:0]
Parity	Command (n+1) valid	Command (n+1)	Reserved	Command (n)

FIGURE 22

2300

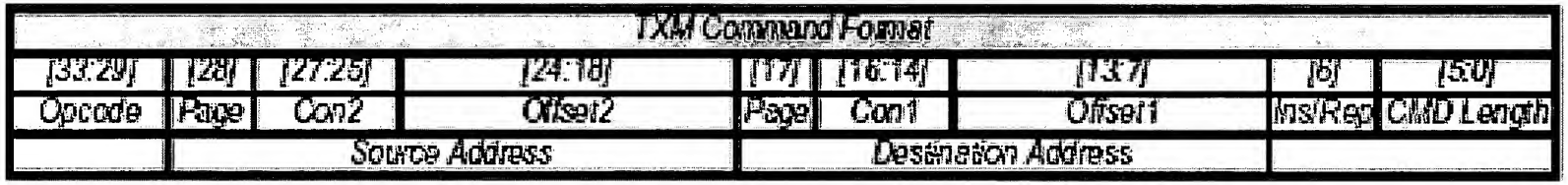


FIGURE 23

Context	Context Name	Location
C0	NULL	The very first byte of the packet including AFH
C1	L2	The start of the MAC header
C2	Ethertype	The start of the Ethertype field (if present)
C3	MPLS	The start of the MPLS header(s) (if present)
C4	L3 Outer	The start of the outer L3 header
C5	L3 Inner	The start of the inner L3 header
C6	L4	The start of the TCP/UDP/? Header

FIGURE 24

Opcode	Command Mnemonic	Control Information	Data Fields
00000	TXM_CMD_NOP	-	-
00001	TXM_CMD_INSERT	Offset, Length	Insertion Data
00010	TXM_CMD_DELETE	Offset, Length	-
00011	TXM_CMD_REPLACE	Offset, Length	Replacement Data
00100	TXM_CMD_REPLACE_MASK	Offset, Length	Replacement Data/Mask
00101	TXM_CMD_COPY	Offset Source, Offset Destination, Length	-
00110	TXM_CMD_COPY_MASK	Offset Source, Offset Destination, Length	Copy Mask
00111	TXM_CMD_COPY_INS	Offset Source, Offset Destination, Length	-
01000	TXM_CMD_COPY_INS_MASK	Offset Source, Offset Destination, Length	Copy Mask
01001	TXM_CMD_MACRO1	VDEL, MCAST flags, MAC DA, MAC SA, VLAN	MAC DA, MAC SA
01010	TXM_CMD_MACRO2	VDEL, MCAST flags, MAC DA, MAC SA, VLAN	MAC DA, MAC SA
01011 - 01100	RESERVED	-	-
01101	TXM_CMD_ACL	Index, VPORT	-
01110	TXM_CMD_EMC_VPRI	VPRI-EXP EMC fields	-
01111	TXM_CMD_EMC_IPTOS	IPTOS EMC fields	-
10000	TXM_CMD_INCREMENT_INSERT	Offset, Length	-
10001	TXM_CMD_INCREMENT_REPLACE	Offset, Length	-
10010	TXM_CMD_DECREMENT	Offset, Length	-
10011	TXM_CMD_AND	Offset, Length	ALU Data
10100	TXM_CMD_OR	Offset, Length	ALU Data
10101	TXM_CMD_XOR	Offset, Length	ALU Data
10110	TXM_CMD_ADD	Offset, Length	ALU Data
10111	TXM_CMD_SUB	Offset, Length	ALU Data
11000	TXM_TTL_DECREMENT	MCAST/BCAST flags	TTL decrement limit registers
11001	TXM_TC_INCREMENT	-	TC limit register
11010	TXM_TTL_DECREMENT_INS	MCAST/BCAST flags	TTL decrement limit registers
11011	TXM_TC_INCREMENT_INS	-	TC limit register
11100 - 11111	Reserved	-	-

FIGURE 25

	txmi_cmd_replace_da	(Context: L2, Offset: 0, Length 6)
	txmi_cmd_data	MAC DA (6 bytes external)
OPT1:	txmi_cmd_replace	(Context: L2, Offset: 6, Length 6)
	txmi_data	MAC SA (6 bytes external)
OPT2:	txmi_cmd_replace_sa	(Context: L2, Offset: 6, Length 6)
	txmi_data	Internal SA Pointer
OPT3:	txmi_cmd_vlan_delete_replace	(Context: L2, Offset: 14, Length 2)
	txmi_data	VLAN (2 bytes external)

OPT1: If configuration register flag (use_interal_mac_sa) is set to 0 then the MAC SA will be read from the external TXM RAM.
OPT2: If configuration register flag (use_interal_mac_sa) is set to 1 then the MAC SA data will come from the internal register in the source field of the command (0 – 15).
OPT3: If the VDEL flag is set to 1 the VLAN field will be deleted else the VLAN field will be replaced with external TXM data.

FIGURE 26

	txmi_cmd_replace_da	(Context: L2, Offset: 0, Length 6)
	txmi_cmd_data	MAC DA (6 bytes external)
OPT1:	txmi_cmd_replace	(Context: L2, Offset: 6, Length 6)
	txmi_data	MAC SA (6 bytes external)
OPT2:	txmi_cmd_replace_sa	(Context: L2, Offset: 6, Length 6)
	txmi_data	Internal SA Pointer
OPT3:	txmi_cmd_vlan_delete	(Context: L2, Offset: 14, Length 2)

OPT1: If configuration register flag (use_interal_mac_sa) is set to 0 then the MAC SA will be read from the external TXM RAM.

OPT2: If configuration register flag (use_interal_mac_sa) is set to 1 then the MAC SA data will come from the internal register in the source field of the command (0 – 15).

OPT3: If the VDEL flag is set to 1 the VLAN field will be deleted else the txmi_cmd_vlan_delete command will be converted to a txmi_cmd_nop command.

FIGURE 27

```
if broadcast IP packets
      if (TTL>IPbcast_TTL_Limit[sub_channel])
            Decrement TTL
            continue with next operation
      else
            Drop the packet
else if multicast IP packets
      if (TTL>IPmcast_TTL_Limit[sub_channel])
            Decrement TTL
            continue with next operation
      else
            Drop the packet
else // Must be unicast IP packets
      if (TTL>Ibucast_TTL_Limit[sub_channel])
            Decrement TTL
            continue with next operation
      else
            Drop the packet
```

FIGURE 28

```
if (TC<TC_Limit[sub_channel])
            Increment TTL

      continue with next operation
else
      Drop the packet
```

FIGURE 29

TXM Command Format for the Tx ACL block			
[33:29]	[28:20]	[19:4]	[3:0]
Opcode	Reserved	VPORT	Index

FIGURE 30

TXM Command Format for the Tx Post Processor block		
[33:29]	[28:8]	[7:0]
Opcode	VPRI-EXP / IPTOS EMC Command	Reserved

FIGURE 31

Error Flag	Error Description	Action
0	ALU & Copy commands > packet size	Flag packet to be killed
1	Destination address is ahead of current read pointer	Flag packet to be killed
2	ALU & Copy commands > packet size	Flag packet to be killed
3	Reserved Opcode detected in the pipeline	Flag packet to be killed
4	Context1 < Context0	Flag packet to be killed
6	Context2 < Context1	Flag packet to be killed
7	Context3 < Context2	Flag packet to be killed
8	Context4 < Context3	Flag Packet to be killed
9	Context5 < Context4	Flag packet to be killed
10	Context6 < Context5	Flag packet to be killed
11	TTL < limit or TC > limit	Flag packet to be killed
12	TXM_IN_DATA_RAM Parity Error	Flag packet to be killed
13	Tx Workbuf Parity Error	Flag packet to be killed
14	TRAM or Internal Recipe RAM Parity Error	Flag packet to be killed
15	Packet modification > 0x80	Flag packet to be killed

FIGURE 32

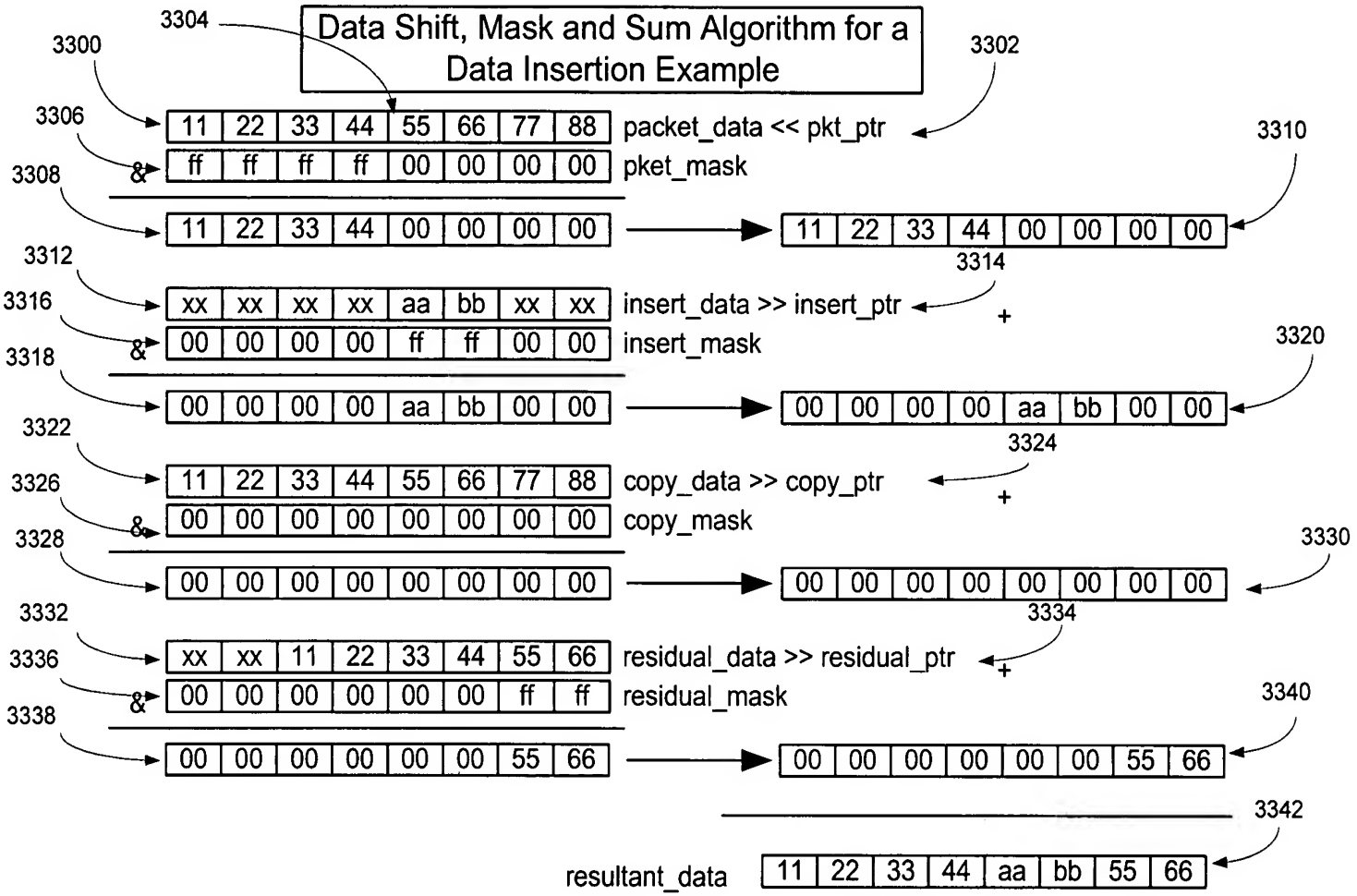

Data Shift, Mask and Sum Algorithm for a Data Insertion Example
3304
3300
3302
3306
3308
3310
3312
3314
3316
3318
3320
3322
3324
3326
3328
3330
3332
3334
3336
3338
3340
3342
11 22 33 44 55 66 77 88
packet_data << pkt_ptr
ff ff ff ff 00 00 00 00
pket_mask
11 22 33 44 00 00 00 00
xx xx xx xx aa bb xx xx
insert_data >> insert_ptr
00 00 00 00 ff ff 00 00
insert_mask
00 00 00 00 aa bb 00 00
11 22 33 44 55 66 77 88
copy_data >> copy_ptr
00 00 00 00 00 00 00 00
copy_mask
00 00 00 00 00 00 00 00
xx xx 11 22 33 44 55 66
residual_data >> residual_ptr
00 00 00 00 00 00 ff ff
residual_mask
00 00 00 00 00 00 55 66
resultant_data
11 22 33 44 aa bb 55 66

FIGURE 33

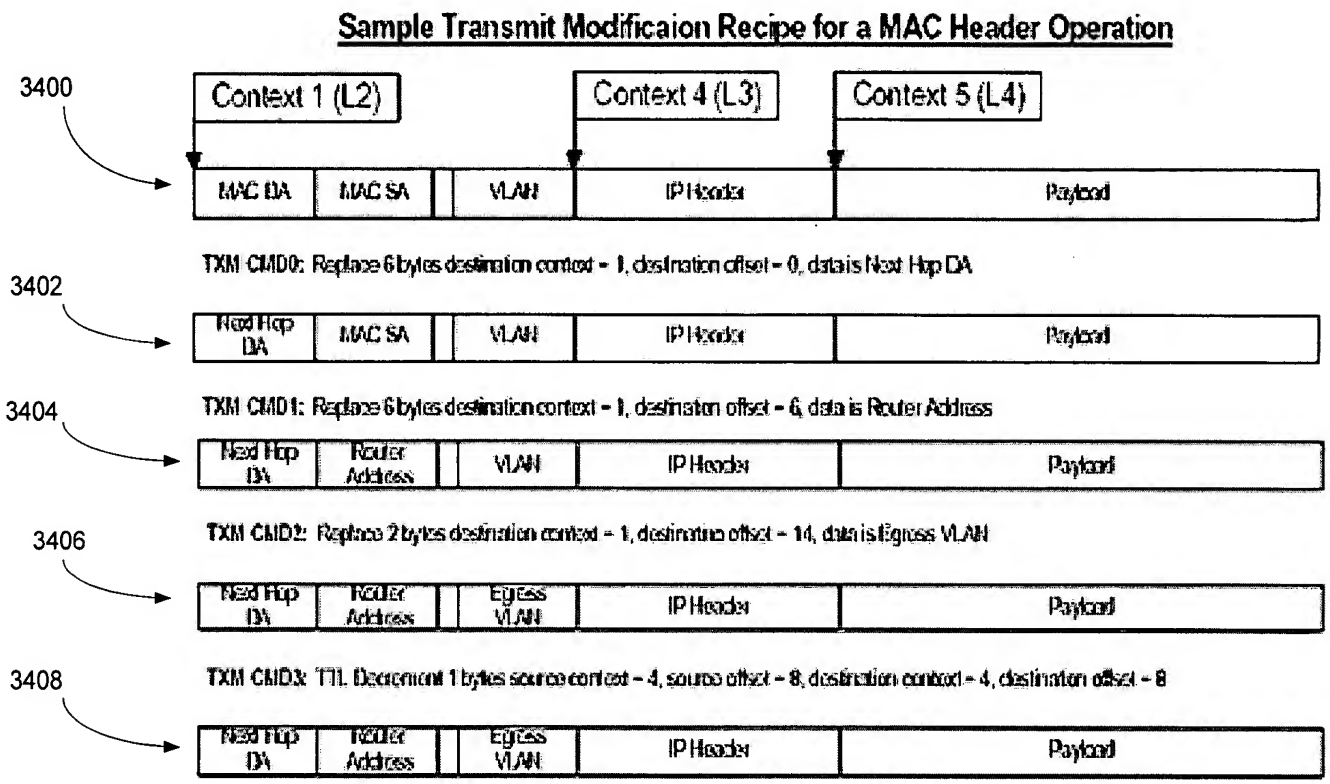

Sample Transmit Modificaion Recipe for a MAC Header Operation
3400
Context 1 (L2)
Context 4 (L3)
Context 5 (L4)
MAC DA
MAC SA
VLAN
IP Header
Payload
TXM CMD0: Replace 6 bytes destination context = 1, destination offset = 0, data is Next Hop DA
3402
Next Hop DA
MAC SA
VLAN
IP Header
Payload
TXM CMD1: Replace 6 bytes destination context = 1, destination offset = 6, data is Router Address
3404
Next Hop DA
Router Address
VLAN
IP Header
Payload
TXM CMD2: Replace 2 bytes destination context = 1, destination offset = 14, data is Egress VLAN
3406
Next Hop DA
Router Address
Egress VLAN
IP Header
Payload
TXM CMD3: TTL Decrement 1 bytes source context = 4, source offset = 8, destination context = 4, destination offset = 8
3408
Next Hop DA
Router Address
Egress VLAN
IP Header
Payload

FIGURE 34

Forwarding Process Operation	Modification Type	Size (Bytes)	Packet Offset(s)
Next Hop MAC DA Replacement	Replace	6	0 (MAC)
Next Hop VLAN ID Replacement	Masked Replace	2	12 (MAC)
Source Address Insertion	Replace	6	6 (MAC)
TTL Decrement IPV4	Decrement	1	8 (NETWORK)
MPLS Stack Single Entry Add/Delete	Insert / Delete	4	0 (MPLS)
MPLS Stack Double Entry Add/Delete	Insert / Delete	8	0 (MPLS)
MPLS Label Change	Replace (could be masked to preserve CoS bits)	4	0 (MPLS)
MPLS TTL Decrement	Decrement	1	3 (MPLS)
MPLS TTL Copy	Copy	1	3 (MPLS) to 8 (NETWORK)
MPLS EtherType Replace/Restore	Replace	2	0 (LLC)
IP v4 Encapsulate/De-Encapsulate	Insert / Delete	20	0 (NETWORK)

FIGURE 35

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	–	–	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	–	–	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14 (no DID)	2
		TXM_CMD_DATA	--	--	–	–	2
TTL Decrement IPv4	4	TXM_CMD_DECREMENT	L3	8	L3	8	1

FIGURE 36

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	–	–	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	–	–	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	–	–	2
Ipv4 Encap	4	TXM_CMD_INSERT	--	--	L3 Outer	0	7
		TXM_CMD_DATA	--	--	–	–	7
TTL Decrement	5	TXM_CMD_DECREMENT INSERT	L3 Outer	8	L3 Outer	0	1
IPv4 Encap	6	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	–	–	8
IPv4 Encap	7	TXM_CMD_INSERT	--	--	L3 Outer	0	4
		TXM_CMD_DATA	--	--	–	–	4

FIGURE 37

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	-	--	L2	0	6
		TXM_CMD_DATA	-	--	--	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	-	--	L2	6	6
		TXM_CMD_DATA	-	--	--	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	-	--	L2	14 (no DID)	2
		TXM_CMD_DATA	-	--	--	-	2
IPV4 de-encapsulate	4	TXM_CMD_DELETE	-	--	L3 Outer	0	0
Decrement Inner TTL	5	TXM_TTL_DECREMENT	L3 Inner	8	L3 Inner	8	1

FIGURE 38

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	-	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	-	-	2
Ipv6 Encap	4	TXM_CMD_INSERT	--	--	L3 Outer	0	7
		TXM_CMD_DATA	--	--	-	-	7
TTL Decrement	5	TXM_CMD_DECREMENT INSERT	L3 Outer	8	L3 Outer	0	1
Ipv6 Encap	6	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	-	-	8
Ipv6 Encap	7	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	-	-	8
Ipv6 Encap	8	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	-	-	8
Ipv6 Encap	9	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	-	-	8

FIGURE 39

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	–	–	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	–	–	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	–	–	2
Ipv6 Encap	4	TXM_CMD_INSERT	--	--	L3 Outer	0	7
		TXM_CMD_DATA	--	--	–	–	7
TTL Decrement	5	TXM_CMD_DECREMENT INSERT	L3 Outer	8	L3 Outer	0	1
IPv6 Encap	6	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	–	–	8
Ipv6 Encap	7	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	–	–	8
Ipv6 Encap	8	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	–	–	8
IPv6 Encap	9	TXM_CMD_INSERT	--	--	L3 Outer	0	8
		TXM_CMD_DATA	--	--	–	–	8

FIGURE 40

CMD Function	CMD #	TXMI CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Last Hope Route Address	1	TXMI_CMD_COPY	L3	10	L2	0	6
Replace MAC SA	2	TXMI_CMD_REPLACE	--	--	L2	6	6
		TXMI_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXMI_CMD_REPLACE	--	--	L2	14	2
		TXMI_CMD_DATA	--	--	-	-	2
Increment TC	4	TXMI_CMD_INCREMENT	L3	5	L3	5	1

FIGURE 41

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	-	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	-	-	2
Replace EtherType	4	TXM_CMD_REPLACE	--	--	Ether	0	2
MPLS Label Insert	5	TXM_CMD_INSERT	--	--	MPLS	0	3
		TXM_CMD_DATA	--	--	-	-	3
TTL Decrement	6	TXM_CMD_DECREMENT	L3	8	MPLS	3	1

FIGURE 42

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	-	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	-	-	2
Replace EtherType	4	TXM_CMD_REPLACE	--	--	Ether	0	2
MPLS Label Insert	5	TXM_CMD_INSERT	--	--	MPLS	0	3
		TXM_CMD_DATA	--	--	-	-	3
TTL Decrement	6	TXM_CMD_DECREMENT	L3	8	MPLS	3	1
MPLS Label Insert	7	TXM_CMD_INSERT	--	--	MPLS	4	3
TTL Decrement	8	TXM_CMD_DECREMENT	L3	8	MPLS	7	1

FIGURE 43

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	-	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	-	-	2
MPLS Label Insert	4	TXM_CMD_INSERT	--	--	MPLS	0	3
		TXM_CMD_DATA	--	--	-	-	3
TTL Decrement	5	TXM_CMD_DECREMENT	L3	8	MPLS	3	1

FIGURE 44

CMD Function	CMD #	TXM CMD MNEUMONIC	Source Context	Source Offset	Destination Context	Destination Offset	Length
Replace MAC DA	1	TXM_CMD_REPLACE	--	--	L2	0	6
		TXM_CMD_DATA	--	--	-	-	6
Replace MAC SA	2	TXM_CMD_REPLACE	--	--	L2	6	6
		TXM_CMD_DATA	--	--	-	-	6
Replace VLAN ID	3	TXM_CMD_REPLACE	--	--	L2	14	2
		TXM_CMD_DATA	--	--	-	-	2
TTL Decrement	4	TXM_CMD_DECREMENT	L3	8	L3	8	1
Replace IP DA or SA	5	TXM_CMD_REPLACE	L3	12/16	L3	12/16	4
		TXM_CMD_DATA	--	--	-	-	4
Replace TCP/UDP Source or Dest port	5	TXM_CMD_REPLACE	L4	0/2	L4	0/2	2
		TXM_CMD_DATA	--	--	-	-	2

FIGURE 45

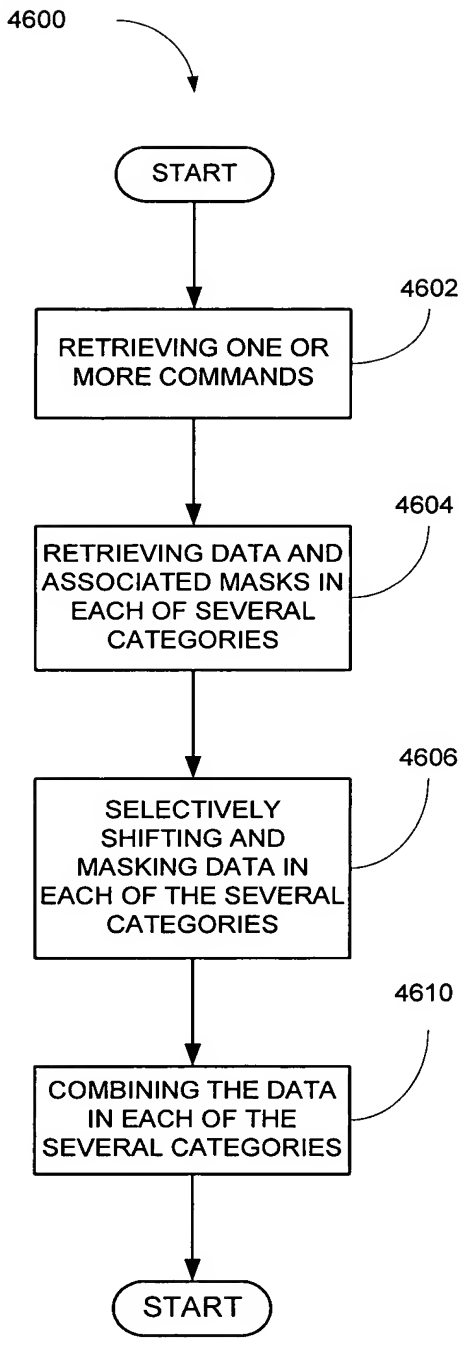

4600
START
4602
RETRIEVING ONE OR MORE COMMANDS
4604
RETRIEVING DATA AND ASSOCIATED MASKS IN EACH OF SEVERAL CATEGORIES
4606
SELECTIVELY SHIFTING AND MASKING DATA IN EACH OF THE SEVERAL CATEGORIES
4610
COMBINING THE DATA IN EACH OF THE SEVERAL CATEGORIES
START

FIGURE 46

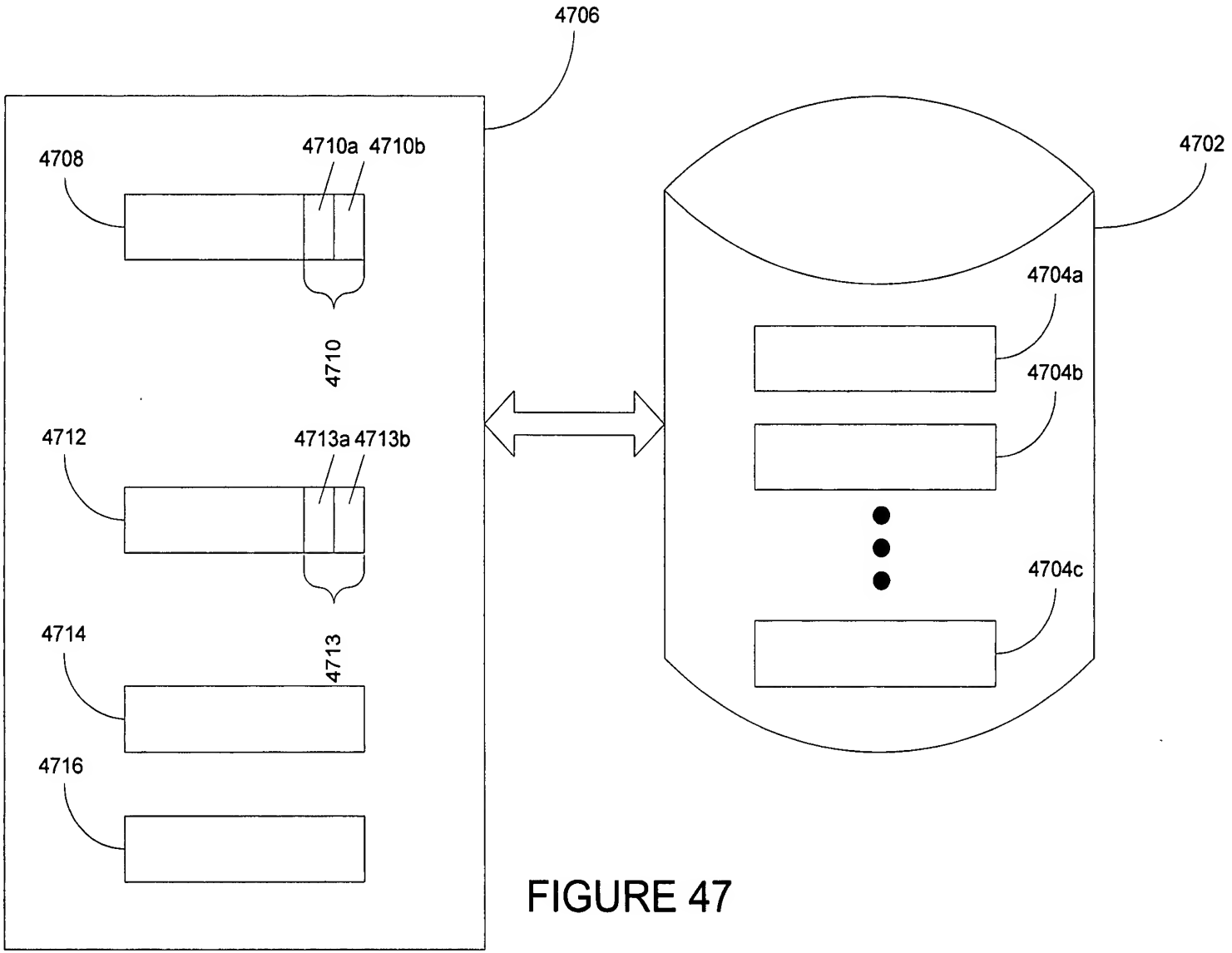

4706
4708
4710a
4710b
4710
4712
4713a
4713b
4713
4714
4716
4702
4704a
4704b
4704c

FIGURE 47

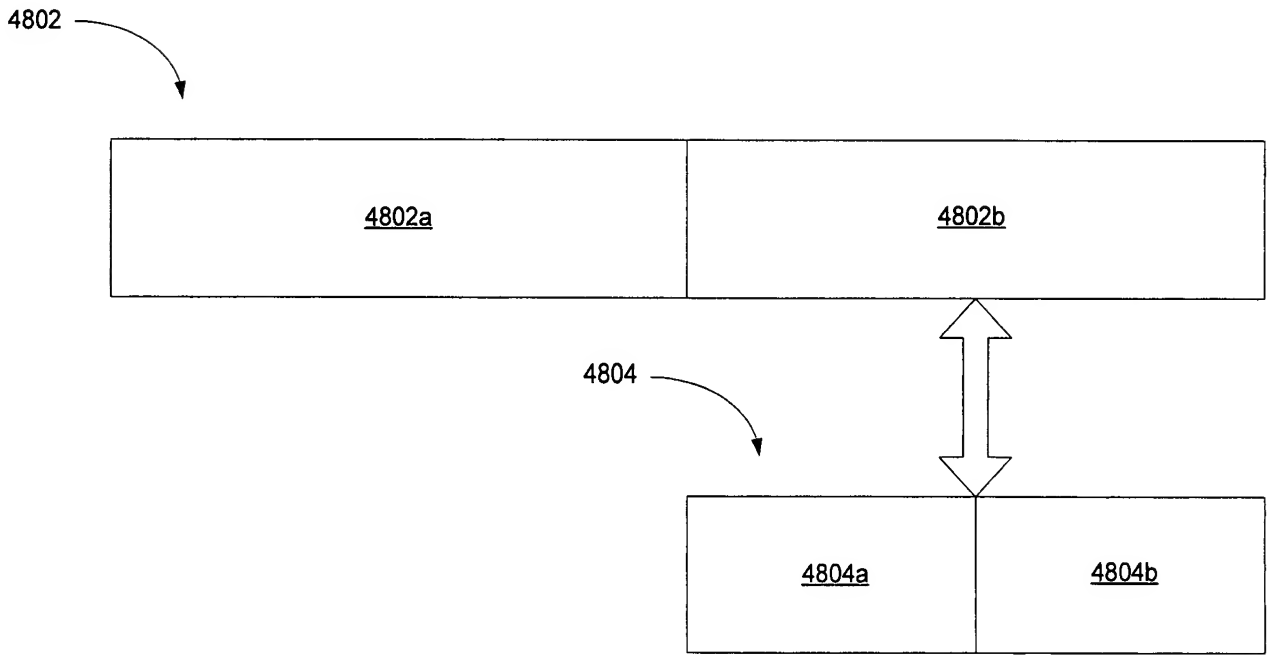


FIGURE 48

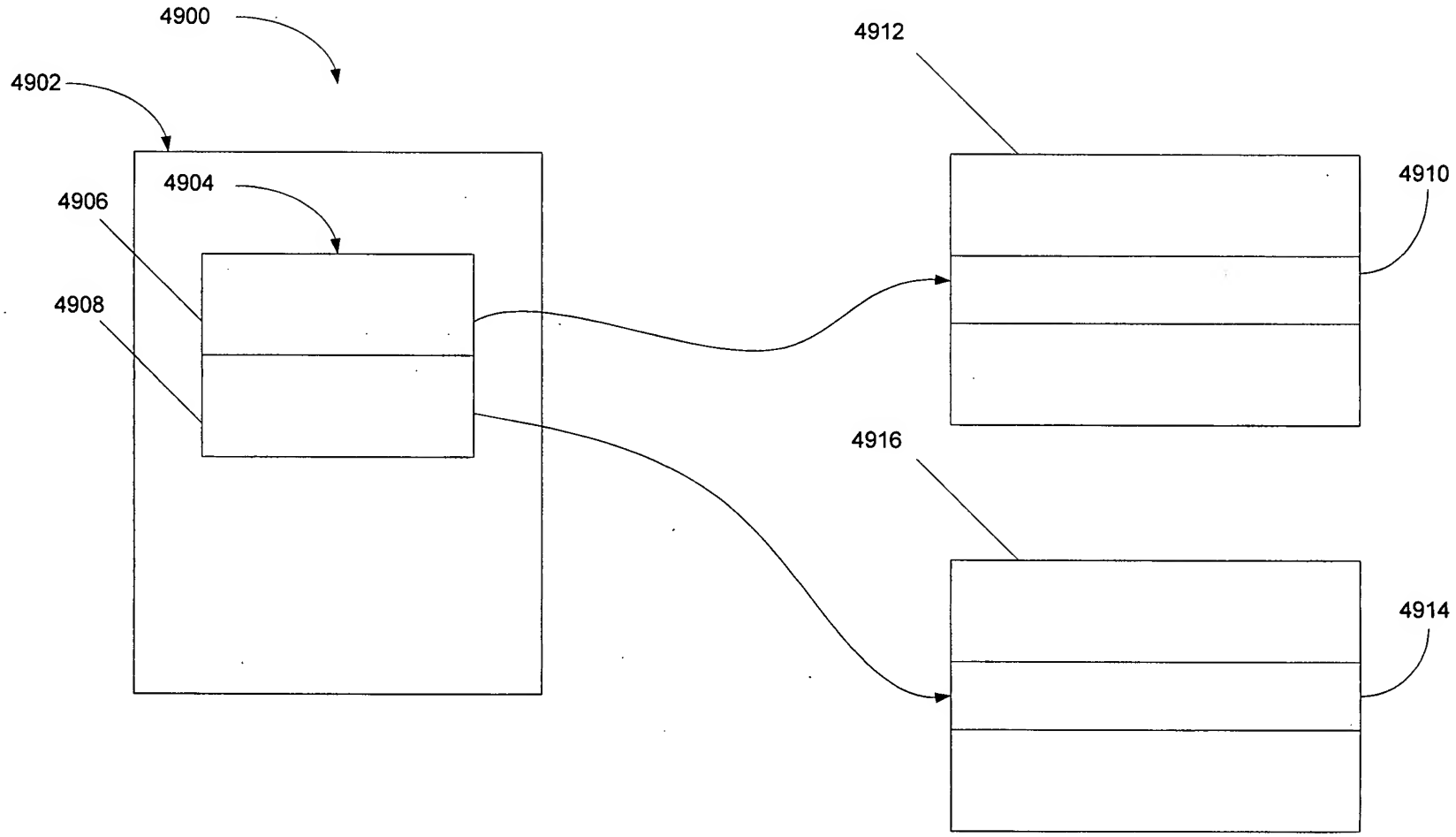


FIGURE 49

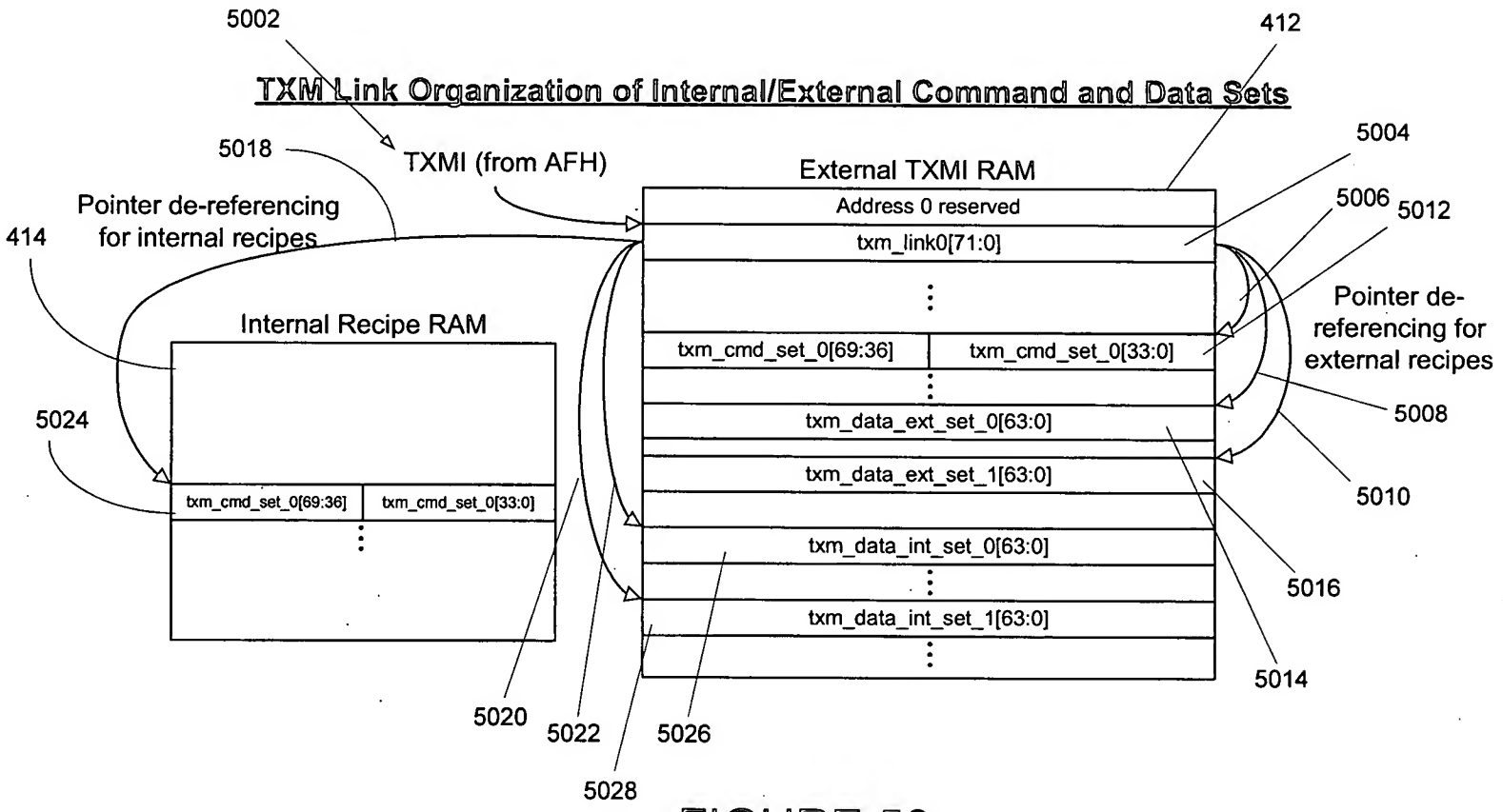

5002
412
TXM Link Organization of Internal/External Command and Data Sets
5018
TXMI (from AFH)
External TXMI RAM
5004
Pointer de-referencing
for internal recipes
414
Address 0 reserved
5006
5012
txm_link0[71:0]
Pointer de-
referencing for
external recipes
Internal Recipe RAM
txm_cmd_set_0[69:36]
txm_cmd_set_0[33:0]
5024
txm_data_ext_set_0[63:0]
5008
txm_data_ext_set_1[63:0]
5010
txm_data_int_set_0[63:0]
5016
txm_data_int_set_1[63:0]
5014
5020
5022
5026
5028

FIGURE 50

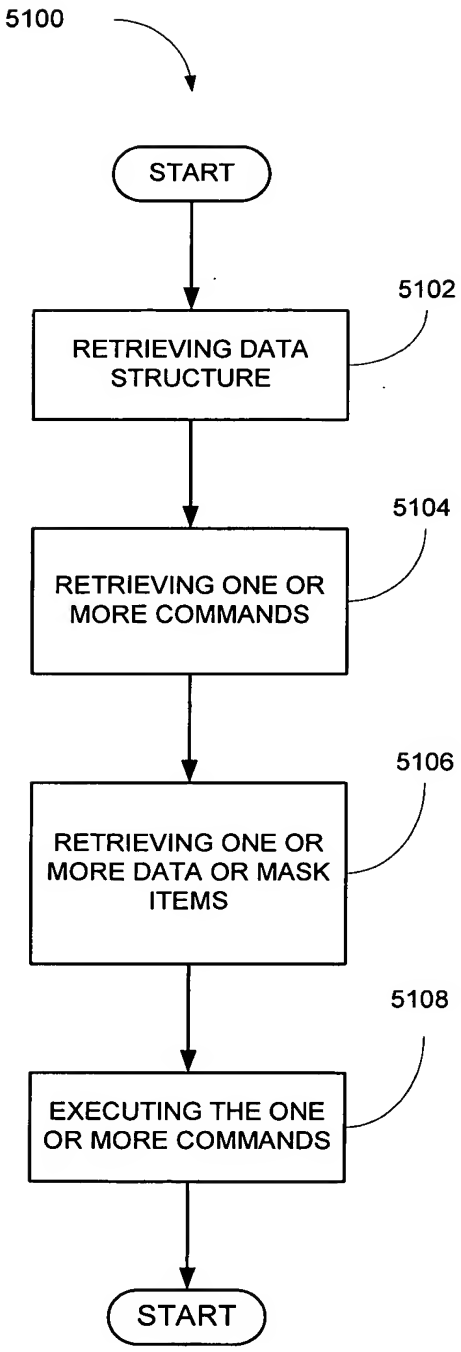

5100
START
5102
RETRIEVING DATA STRUCTURE
5104
RETRIEVING ONE OR MORE COMMANDS
5106
RETRIEVING ONE OR MORE DATA OR MASK ITEMS
5108
EXECUTING THE ONE OR MORE COMMANDS
START

FIGURE 51

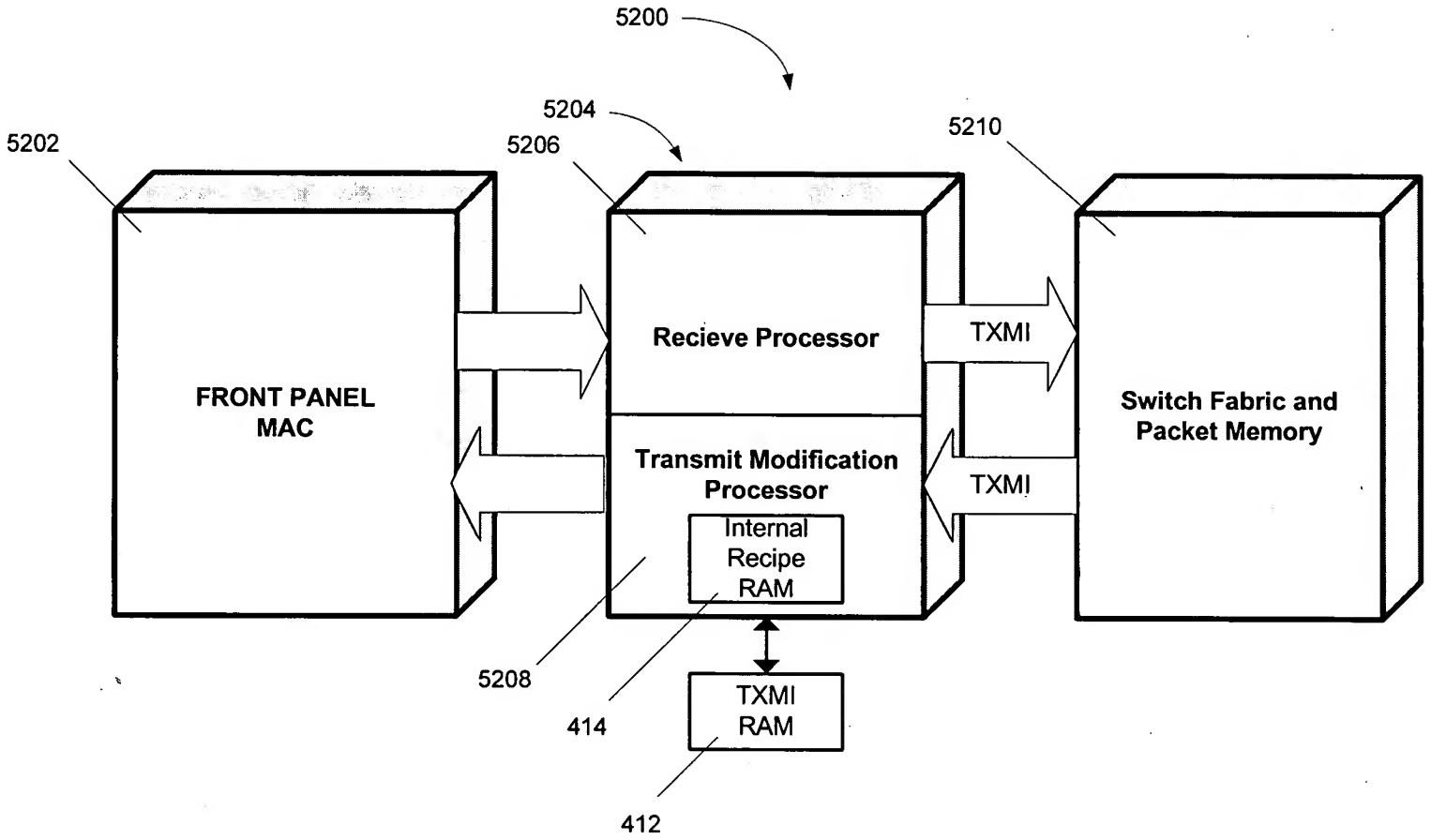

5200
5204
5202
5206
5210
FRONT PANEL
MAC
Recieve Processor
TXMI
Switch Fabric and
Packet Memory
Transmit Modification
Processor
TXMI
Internal
Recipe
RAM
5208
414
TXMI
RAM
412

FIGURE 52